UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/638,245	08/14/2000	Christopher M. Hanna	56233-139 (THTK-3DVCN0)	1379

23630 7590 11/07/2012

McDermott Will & Emery
The McDermott Building
500 North Capitol Street, N.W.
Washington, DC 20001

EXAMINER	
LEE, PING	

ART UNIT	PAPER NUMBER
2654	

NOTIFICATION DATE	DELIVERY MODE
11/07/2012	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mweipdocket@mwe.com

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/638,245
Filing Date: August 14, 2000
Appellant(s): HANNA, CHRISTOPHER M.

G. Matthew McCloskey
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 30, 2012 appealing from the Office action mailed September 29, 2011.

(1) Grounds of Rejection to be Reviewed on Appeal

Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

The following ground(s) of rejection are applicable to the appealed claims:

1.1. Claims 69-71,78-87, 89-93, 106, 109, 110, 115, 117, 119, 134-174 and 176-184 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson et al. (hereafter Gibson; US 4,760,602) in view of the prior art as shown in Fig. 1 (hereafter AAPA).

Regarding claim 86, Gibson discloses a BTSC processor for L-R signal at the transmitter (shown in Fig. 1A; col. 2, lines 56-60; col. 1, lines 5-24) and a BTSC processor at the receiver (shown in Fig. 1 B). The adaptive weighting circuit could be implemented in analog or digital form (col. 8, lines 11-16). Thus, Gibson meets the claimed limitation as specified in B.

Gibson fails to show the processor for L+R signal at the transmitter. However, BTSC encoder at the transmitter inherently includes processor for processing L+R signal. See col. 3, line 1 of Gibson. AAPA is cited here to clearly illustrate a processor for processing L+R signal and another processor for processing L-R signal. As illustrated in AAPA, the processor for processing L+R signal is simpler than the

processor for processing L-R signal (see also in the background, p. 5, line 3+ of the instant application). By using digital circuit for implementing a digital processor for processing L-R signal (with more complex design involved) as suggested in Gibson, one skilled in the art could expect that a digital processor could be designed for processing L+R signal (with less complex design comparing with processing L-R) without undue experience.

Gibson teaches that L-R signal is in a general sampled data form (col. 8, line 13). Nevertheless, Gibson fails to explicitly teach how to do so. Thus, one skilled in the art would have expected that any well-known method for converting and sampling the left and right signals could be used. Examiner takes Official Notice that this feature is notoriously well known in the art. The sampled left and right signals would form the digital L+R signal and the digital L-R signal.

The limitation as defined in D is a functional statement. By providing the structure as claimed, this limitation is inherently met according to BTSC standard that complies by Gibson and AAPA. Furthermore, by processing the sum signal and the difference signal in parallel simultaneously, but with different circuit elements (see AAPA), one skilled in the art would have expected that the conditioned sum signal may not be in the same phase as the conditioned difference signal. In other words, if they are being processed by the exact same circuit elements, their phases are expected to be matched. Gibson explicitly teaches that matching delays and synchronizing latches may be required (col. 8, lines 16-21). Such elements are eliminated from illustration in Gibson because Gibson wanted to simplify the illustration. Thus, Gibson implies that it

is within the level of ordinary skill in the art to use delays and latches when the need is arise in order to synchronize and match the signals.

Thus, by suggested in Gibson to digitally process L-R using the more complex operation, it would have been obvious to one of ordinary skill in the art to combine Gibson and AAPA by designing a digital processor for L+R signal and a digital processor for L-R in order to process both the L+R signal and the L-R in digitized form and enjoy the same benefit such as noise reduction comparing with using amplifiers in analog circuit.

Regarding claims 87 and 115, the claimed system, comparing with claim 86, further includes a digital composite modulator. Gibson teaches a modulator (col. 2, line 65+). As discussed in claim 86, the L+R signal and the L-R signal are digitally processed. L+R signal or the L-R signal is a digital composite signal. So the modulator used for modulating the digital L+R signal and the digital L-R signal could read on the claimed digital composite modulator. The limitation that the BTSC encoder has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard is a function statement. This feature is an inherent feature when one skilled in the art designs the digital processor for processing L+R signal and the digital processor for processing L-R signal as specified as the BTSC encoder.

Claim 89 is similar to claim 86.

Regarding claim 90, Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are included in

a single integrated circuit. When an engineer designs a system, the size of the system is a very important factor to be considered due to the cost of manufacturing, shipping, weight, and overall appearance of the product. With the advanced technology, the size of an electronic circuit, in general, has reduced dramatically. Thus, it would have been obvious to one of ordinary skill in the art to modify the combination of Gibson and AAPA to try to placing the digital matrix unit, the difference channel processing unit, and the sum channel processing unit in a single integrated circuit in order to reduce the cost of the system and make a smaller system.

Regarding claim 91, Gibson and AAPA fail to show that the digital matrix unit, the difference channel processing unit, and the sum channel processing unit are implemented by a DSP. Gibson suggests a general digital circuitry. Examiner takes Official Notice that using a DSP to perform the digital processing function is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by using well known DSP in order to program the DSP to perform the digitized encoding function.

Regarding claims 69, 70, 78, 79, 80, 81, Gibson further fails to show a digital-to-analog converter arrangement. By digitally processing the L+R signal and the L-R signal, they are digitally encoded signals. Gibson teaches a general modulator (col. 2, lines 65+). A general analog modulator or a general digital modulator is well known in the art. With a general analog modulator, the digitally processed L+R signal and the digitally processed L-R signal have to be converted to analog format in order to be transmitted by the analog modulator. That is, DACs are at the inputs of a general

analog modulator. On the other hand, when using a digital modulator, a DAC, at the output of the digital modulator, could be used to convert the modulated digital signal to analog signal. Examiner takes Official Notice that DAC is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by including well-known DAC in order to use the analog modulator to combine the digitally processed L+R signal and L-R signal, or using well-known DAC for converting the digitally modulated composite signal.

Regarding claims 71, the claimed "preselected sample rate" is inherently included in a digital signal.

Regarding claims 82, 83 and 85, the limitation specified in this claims has been discussed in claim 86 above.

Regarding claim 84, the claimed 75 μs reemphasis is inherently included according to BTSC standard.

Regarding claim 92, comparing with claim 87 discussed above, Gibson fails to show that the matrix unit has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard. The function of the matrix unit is to generate a L+R signal and a L-R signal. The AAPA discloses a matrix unit. This matrix unit could be easily designed to generate a digital L+R signal and a digital L-R signal without undue experience. The frequency response of the digital matrix unit should be similar to the frequency response of the equivalent analog matrix unit in order to preserve the signal contents (sum and difference signals). Examiner takes Official Notice that this feature is notoriously well known in the art. By

using such matrix unit, the digital L-R signal could be processed by the digital processing unit as suggested in Gibson. Using a digital matrix has been discussed in claim 86 above.

Regarding claim 93, the claimed frequency is an inherent feature of a BTSC broadcasting signal.

Regarding claims 106 and 117, the limitations in the claims are similar to those in claims 86 and 87 with the exception of the adaptive signal weighting system configured to dynamically vary the phase of the digital difference signal, and the digital sum channel section comprising one or more digital filters for altering the phase of the digital sum signal. Gibson hints that the adaptive network for processing the difference signal would inherently vary the phase (col. 2, lines 12-18). Gibson also teaches that matching delays and synchronizing latches may be required between particular circuit elements which would be known to those in the art (col. 8, lines 17-19) when implementing the digital version of the adaptive filter network. Although Gibson's suggestion is not directly toward the digital sum channel section, Gibson's suggestion applies to all circuit sections that require synchronization. The stereophonic signal to be broadcasted using BTSC encoder requires synchronization between the processed L+R signal and the processed L-R signal. Thus, it would have been obvious to one of ordinary skill in the art to further modify the combination of Gibson and AAPA by including necessary delays in the digital sum channel section and/or delay in the digital difference channel section in order to provide synchronized L-R signal and the L+R signal to the modulator.

Regarding claims 109 and 119, the limitations in the claims are similar to those in claims 86 and 87 with the exception of the digital signal processor has a frequency response in the digital domain that is substantially equal to the analog frequency response specified by the BTSC standard. As discussed above, Gibson suggests that the variable preemphasis network, which processes the L-R signal, could be implemented in either analog or digital form. Gibson does not emphasis whether one should use a digital variable preemphasis network or the analog one. Thus, one skilled in the art would have reasonably concluded that they are functionally equivalent, hence, they produce similar result. The frequency response of the digital variable preemphasis network would have been substantially equal to the analog preemphasis network. The circuit for processing L+R signal is simple and straight forward comparing with the circuit for processing L-R signal (see Fig. 1 of AAPA; this has been discussed for claim 86 above). When Gibson suggests digital variable preemphasis network, one could design and implement in digital circuit for processing L+R signal as well without undue experience. As with the digital for processing the L-R signal, one skilled in the art would have reasonably concluded that the digital circuit for processing L-R signal should be functionally equivalent to the analog circuit, hence, they produce similar result. The frequency response of the digital circuit for L+R would have been substantially equal to the analog circuit for L+R. The same logic applied to the combining section as well.

Claim 110 is similar to claim 109.

New claims 134-174 and 176-183 are substantially in the same form as claims 60-93, 106,109,112-115, 117 and 119 which have been discussed above.

1.2. Claims 60-68, 72-77, 88 and 112-114 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gibson and AAPA as applied to claims 69-71,78-87, 89-93, 106, 109, 110, 115, 117, 119, 130-174 and 176-183 above, and further in view of Crochiere et al. (hereafter Crochiere) ("Interpolation and Decimation of Digital Signals - A Tutorial Review").

Regarding claims 88, 72-77, Gibson and AAPA fail to show a first up-sampler configured to insert additional samples into the summations signal to increase the sample rate of the summation signal and a second up-sampler configured to insert additional samples into the difference signal to increase the sample rate of the difference signal. Crochiere teaches sampling general digital signals. According to Crochiere, the sampling rate is a fundamental consideration of digital signal processing techniques and applications. It determines the convenience, efficiency, and/or accuracy in which the digital signal processing can be performed. The sampling rate can be and should be converted to a different one so the resulting signal corresponding to the same analog function or to convert rate in the system from one rate to another when performing different parts of processing algorithm at different sampling rates (second column of p. 300 and abstract). When the rate needs to increase, Crochiere teaches using interpolation. When the rate needs to decrease, Crochiere teaches using decimation. The analog circuit as shown in AAPA involves many signal processing steps. Specifically, the sum signal and the difference signal are processed separately and fundamentally differently. Thus, with Gibson, AAPA and Crochiere in front of

him/her, it would have been obvious to one of ordinary skill in the art to combine them to form a digital BTSC encoder with necessary interpolator and/or decimator in order to ensure that the digital BTSC encoder would generate a signal that corresponds to the analog signal according to the analog BTSC encoder and the digital BTSC encoder would produce signal with accurate data with great efficiency.

The claimed 75 μs preemphasis is inherently included according to BTSC standard. The claimed "digital signal processor" could also be interpreted as a circuit for processing digital signal. Regarding claims 60, 61, 63-65, 67, 68, Gibson further fails to show a digital-to- analog converter arrangement. By digitally processing the L+R signal and the L-R signal, they are digitally encoded signals. Gibson teaches a general modulator (col. 2, lines 65+). A general analog modulator or a general digital modulator is well known in the art. With a general analog modulator, the digitally processed L+R signal and the digitally processed L-R signal have to be converted to analog format in order to be transmitted by the analog modulator. That is, DACs are at the inputs of a general analog modulator. On the other hand, when using a digital modulator, a DAC, at the output of the digital modulator, could be used to convert the modulated digital signal to analog signal. Examiner takes Official Notice that DAC is notoriously well known in the art. Thus, it would have been obvious to one of ordinary skill in the art to further modify Gibson and AAPA by including well-known DAC in order to use the analog modulator to combine the digitally processed L+R signal and L-R signal, or using well-known DAC for converting the digitally modulated composite signal.

Regarding claims 62, 66 and 75, the claimed "preselected sample rate" is inherently included in a digital signal.

Regarding claims 112-114, the signal transformation arrangement reads on the up sampler which has been discussed with respect to claim 88 above.

(2) Response to Argument

2.1. For claims 69-71, 78-87, 89-93, 106, 109, 11, 115, 117, 119, 134-174 and 176-184.

On p. 97, appellant argued that there is no teaching in Gibson concerning enablement of the digital implementations, i.e., how such implementations are to be practiced. This is not persuasive. A reference is presumed to be operable/enabling. Once such a reference is found, the burden is on applicant to provide facts rebutting the presumption of operability. MPEP 2121, I. Appellant has not provided any factual evidence to prove that Gibson does not provide enablement for digital implementations. Even if a reference discloses an inoperative device, it may qualify as prior art for the purpose of determining obviousness under 35 U.S.C. 103. MPEP 2121, II. Gibson not only suggests digital implementations, Gibson also anticipates the phase disparity between circuit elements and possible data overflow or underflow (col. 8, lines 17-28). Those are the conditions that one skilled in the art would have expected for digital implementations. Appellant stated that Gibson does not describe a single digital embodiment with any specificity. However, claim 86, for example, does not include any specific that differentiates between the invention in claim 86 from the combination of

Gibson and AAPA. For example, claim 86 includes a general difference channel processing section to encode the digital difference signal. It is noticed that no detail/structure is being claimed for the difference channel processing section in claim 86. Gibson suggests a difference channel processing section being digitally implemented. Thus, Gibson meets the limitation of the claimed general difference channel processing section. Appellant stated that it is extremely difficult to match the amplitude and phase responses (p. 99 of the brief) and discussed the difficulty with sections in the specification as originally filed. However, no specific detail/structure has been explicitly stated in the claims that deal with such difficulty. The limitation of the claimed difference channel processing section in claim 86, for example, is a section to encode the digital difference signal according to the BTSC standard. This limitation reads on any digital difference section that encodes the difference signal according to BTSC standard. In view of the teaching in Gibson, it is clear to one of ordinary skill in the art that Gibson meets the limitation of the claimed general difference channel processing section.

On p. 101, applicant argued that the examiner appears to disregards all the limitations in claim 86 when addresses part D. This is not persuasive. Both Gibson and AAPA teach devices that meet BTSC standard. The standard includes the criteria that the difference between the sum signal and difference signal, for a given frequency and level, conforms with the difference specified by the BTSC standard. A device must meet the standard whether the signals are being processed digitally or analogously.

The limitations recited in A, B and C of claim 86 have been analyzed and compared with the combination of Gibson and AAPA and have been shown that they are obvious to one skilled in the art in view of the combination of Gibson and AAPA. Sections A, B and C form the device that meets BTSC standard. Section D in claim 86 is the result/function of a device that meets BTSC standard. When the structures in the claim are shown in the prior art, then the prior art would inherit the inherent function.

On pp. 102-105, in response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

On p. 106, appellant argued that Gibson does not "hint" or otherwise imply or state that an adaptive network processing the difference signal would inherently vary the phase. This is not persuasive. Gibson discussed that it is difficult to match the transfer function and its complementary transfer function. The invention suggested in Gibson would allow one to implement BTSC transfer function without requiring two, closely matched, signal filters. For Fig. 6, Gibson teaches a delay element is added to

vary the phase. On col. 8, lines 17-28, Gibson even suggests that delays and synchronizing latches may be required. Thus, Gibson teaches the claimed adaptive signal weighting system configured to dynamically vary the phase of the digital difference signal.

2.2. For claims 60-68, 72-77, 88 and 112-114.

Appellant's argument referred back to the previous rejection in view of the combination of Gibson and AAPA. In response to applicant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). In this case, Gibson provides the explicitly suggestion, teaching and motivation for digital implementations.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Ping Lee/

Primary Examiner, Art Unit 2654

Conferees:

/Ping Lee/

Primary Examiner, Art Unit 2654

/VIVIAN CHIN/

Supervisory Patent Examiner, Art Unit 2654

/CURTIS KUNTZ/

Supervisory Patent Examiner, Art Unit 2656